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FORM PTO 1390 (Modified) REV 11-98 — U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

DEC 27 2000 PATENT & TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER	
002985.1002	
U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	
09/720782	
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE
PCT/GB99/02060	June 30, 1999
PRIORITY DATE CLAIMED	
June 30, 1998	

TITLE OF INVENTION
RESIDUAL CURRENT DETECTION DEVICE

APPLICANT(S) FOR DO/EO/US
Robert Charles SKERRITT, et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Letter Re Priority

PCTUS1/REV03

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/720782	PCT/GB99/02060	602985.1002

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO **$970.00**	
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO **$840.00**	
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$690.00**	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$670.00**	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$96.00**	

ENTER APPROPRIATE BASIC FEE AMOUNT = **$860.00**

Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)). **$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	- 20 =	0	x	**$0.00**
Independent claims	- 3 =	0	x	**$0.00**
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**

TOTAL OF ABOVE CALCULATIONS = **$860.00**

Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable)**. ☐ **$0.00**

SUBTOTAL = **$860.00**

Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). + **$0.00**

TOTAL NATIONAL FEE = **$860.00**

Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐ **$0.00**

TOTAL FEES ENCLOSED = **$860.00**

Amount to be: refunded $

charged $

☒ A check in the amount of **$860.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **50-0518** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

STEINBERG & RASKIN, P.C.
1140 Avenue of the Americas, 15th Floor
New York, New York 10036-5803

J. David Dainow
SIGNATURE

J. David Dainow
NAME

22,959
REGISTRATION NUMBER

December 27, 2000
DATE

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Robert Charles SKERRITT, et al.**	Docket No. **602985.1002**

Serial No.	Filing Date	Examiner	Group Art Unit
09/720782 N/Y/K	**December 27, 2000**	**N/Y/K**	**N/Y/K**

Invention: **RESIDUAL CURRENT DETECTION DEVICE**

I hereby certify that the following correspondence:

New 371 application based on a PCT application with associated documents and fee

(Identify type of correspondence)

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on

December 27, 2000
(Date)

Annette McPherson
(Typed or Printed Name of Person Mailing Correspondence)

Annette McPherson
(Signature of Person Mailing Correspondence)

EL681780243US
("Express Mail" Mailing Label Number)

Note: Each paper must have its own certificate of mailing.

Residual Current Detection Device

This invention relates to a residual current correction device for use in a circuit breaker.

Conventionally, residual current correction is detected utilising a current transformer having primary windings through which, in the case of a single phase device, load current flows in opposite directions so that if the return current is different from the outwardly flowing current because of current leakage an output voltage signal is induced in a secondary winding of the transformer. In the case of a multi-phase device, primary windings of the transformer are connected in all of the phase lines and the neutral line. In normal situations, when there is no current leakage, the net current in the lines is zero so that no output voltage is zero.

Sophisticated materials have been developed for the core of the current transformer, which enable considerable accuracy to be obtained when the currents flowing in the primary windings are substantially sinusoidal. However, switch mode power supplies are often used for computers and other equipment and there is an increasing tendency for such equipment to cause dc offsets in the currents. Such developments have made detectors utilising current transformers less reliable and prone to false tripping or failure to detect a dc current leak.

This is a particular problem in the case of directly actuated electro-mechanical devices, where the current transformer secondary actually drives an actuator. The situation is not much improved, when by including an electronic detection and amplification means connected to the secondary winding, as there are still problems with high frequency transients and dc offsets. A very small dc current level can cause the core

to saturate thereby seriously impairing the ability of the detector to detect current leakage.

It is an object of the present invention to provide a residual current detection device in which the above mentioned problems are substantially overcome in a simple and efficacious manner.

In accordance with the invention there is provided a residual current detection device comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines though which current can flow to and from a load, and detector means sensitive to the voltage developed across each of the shunts to detect any imbalance between the currents flowing though the shunts.

Preferably, the detector means comprises an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters and determining whether a current imbalance exists.

Each shunt preferably takes the form of a composite strip having conductive portions at its ends and a resistive portion interconnecting the conductive portions. Such composite strips can be mass produced inexpensively to very high tolerances which makes them extremely suitable for this purpose.

The analog to digital converter for each shunt may include a delta-sigma modulator, which generates a high frequency single digital data stream which is converted by decimation filtering to a multibit digital data stream at a lower frequency.

The analog to digital converter for each shunt is preferably connected to

the processor through an isolation barrier so that the converter can float at the voltage level of the shunt which it serves. The decimation filtering may be effected entirely in the converter, entirely in the processor or split between the converter and the processor.

In the accompanying drawings:

Figure 1 is a diagrammatic perspective view of an example of the invention as applied to a single phase device and

Figure 2 is a block diagram of an another example of the invention as applied to a three phase device.

In the device shown in Figure 1, a substrate 10 supports two composite conductor strips 11, 12. Each of these includes end portions 13 of copper and an intermediate portion 14 of a resistive material such as manganin. The strips are formed by slicing up a sandwich formed by electron beam welding the copper portions to opposite sides of the manganin portion. The shunts formed by the resistive portions manufactured by this method can have a nominal resistance of 0.2mΩ to a tolerance of less than 5%. If the two shunts 14 used on one device are pressed from adjacent portions of the sandwich stock, they are matched to within 2%. Calibration of the shunts built into a unit at two different temperatures can virtually eliminate shunt errors.

In the example shown in Figure 1, there is a separate signal pre-processing ASIC 15 mounted on each of the shunts 14 and connected to the copper end portions 13 of the associated conductor strips. The two ASICs 15 are connected to via an isolation transformer array 16 to a main processor 17. The ASICs 15 operate to convert the two voltages across the shunts into a

digital signal stream which is communicated to the processor 17 via the isolation transformer array. The main processor is programmed to provide a drive signal to a trip actuator 18.

Figure 2 shows in rather more electrical detail a three phase device. In this case there are four shunts 14, one in each phase line and a fourth in the neutral line. The ASICs 15 of Figure 1 are shown as four separate blocks 20, 21, 22, and 23, and there is a power supply unit 24 which draws power from the phase lines on the mains side of the shunts 14 and provides controlled voltages to the processor 17. Power is supplied to the four blocks 20 to 23 via isolation barriers 25 which make up the array 16. Each block of the ASIC includes an analog to digital converter in the form of a delta-sigma modulator which provides a high frequency one bit digital data stream. A multiplexer may be included in each converter so that the converter can provide to the processor, through the respective isolation barrier, signals representing both current in the associated shunt and the voltage at one end of it. The processor uses these signals to monitor the current in each shunt and to operate the actuator 18 if an imbalance occurs.

It will be noted that the voltage sensing connections to the ASICs are made via resistor chains connected between each phase line and the neutral. Each such resistor chain comprises an outer pair of precision resistors of relatively low ohmic value and an intermediate resistor of relatively high ohmic value. These resistor chains allow the RCD to be provided with an independent reference. If the neutral ADC is taken as the selected system reference, then the operating software of the main processor can use the multiple signals derived from the several resistor chains to calibrate each phase against the neutral reference.

The CPU is programmed to carry out the necessary calculations to determine the existence of an imbalance and can determine the true RMS value of the residual current, which conventional devices fail to do correctly particularly in the case of non-sinusoidal current waveforms. The CPU may be programmed to enable it to determine from the data it receives whether a particular event is, in fact, an unacceptable leakage more reliably than conventional devices. For example, the CPU can take into account the historic performance of the unit when setting the leakage current threshold and may ignore events which have a recognisable "signature". In this way improved tolerance to nuisance tripping can be obtained

Decimation filtering of the high frequency one bit data stream is required to reduce each data stream to a multi-bit digital signal at a predetermined sample frequency. By way of example, each current signal may be a 23-bit signal at a sample rate of 64 times the mains frequency, but lower resolution at lower sample rates can be employed when non-linear, rather than linear conversion is acceptable. The decimation filtering is typically a function of the processor, filtering of the four data streams being executed simultaneously so that sample values are derived for all four shunts simultaneously.

In alternative embodiments, one or more stages of the decimation filtration may be executed by hardware included within the ASIC. Multi-bit digital words are transmitted serially across the isolation barriers instead of a one-bit signal stream.

The arrangements described enable very accurate detection of current imbalance to be effected even in the presence of switching transients and DC offsets. The problems which arise from potential saturation of the

current transformer core are avoided completely.

Since the CPU receives actual line current and voltage data from each of the blocks 20 to 23, it can be programmed to perform other calculations, such as current limit and power consumption. Thus an RCD device constructed as described above can also provide the functions of a conventional circuit breaker and/or those of a power consumption meter without any additional sensing or analog-to-digital components being required.

ABSTRACT

RESIDUAL CURRENT DETECTION DEVICE

A residual current detection device for detecting current imbalance including a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load, and a detector is provided for each shunt, each of the detectors being sensitive to the voltage developed across the shunt for providing a signal indicative of the current flowing through the shunt, whereby any imbalance between the currents flowing through the shunts can be reached.

CLAIMS

1. A residual current detection device comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load, and respective detector means is provided for each shunt, each of the respective detector means being sensitive to the voltage developed across the shunt for providing a signal indicative of the current flowing through the shunt, whereby any imbalance between the currents flowing through the shunts can be detected.

2. A device as claimed in Claim 1, in which the detector means comprises an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters and determining whether a current imbalance exists.

3. A device as claimed in Claim 1 or Claim 2, in which each shunt takes the form of a composite strip having conductive portions at its ends and a resist portion interconnecting the conductive portions.

4. A device as claimed in Claim 2 or Claim 3, in which the analog to digital converter for each shunt includes a delta-sigma modulator which produces a high frequency signal digital data stream which is converted by decimation filtering into a multi-bit digital data stream at a lower frequency.

5. A device as claimed in Claim 2, 3 or 4, in which each converter is in the form of an integrated circuit mounted on a corresponding one of the resistive shunts.

6. A device as claimed in Claim 5, in which each integrated circuit has analog input terminals connected by lead wires to the two copper end portions of the corresponding one of the resistive shunts.

7. A device as claimed in Claim 6, in which the integrated circuit also has a terminal connected to a voltage reference source and includes a second converter for providing a digital signal stream dependent on the voltage on one of the copper end portions of the associated one of the shunts.

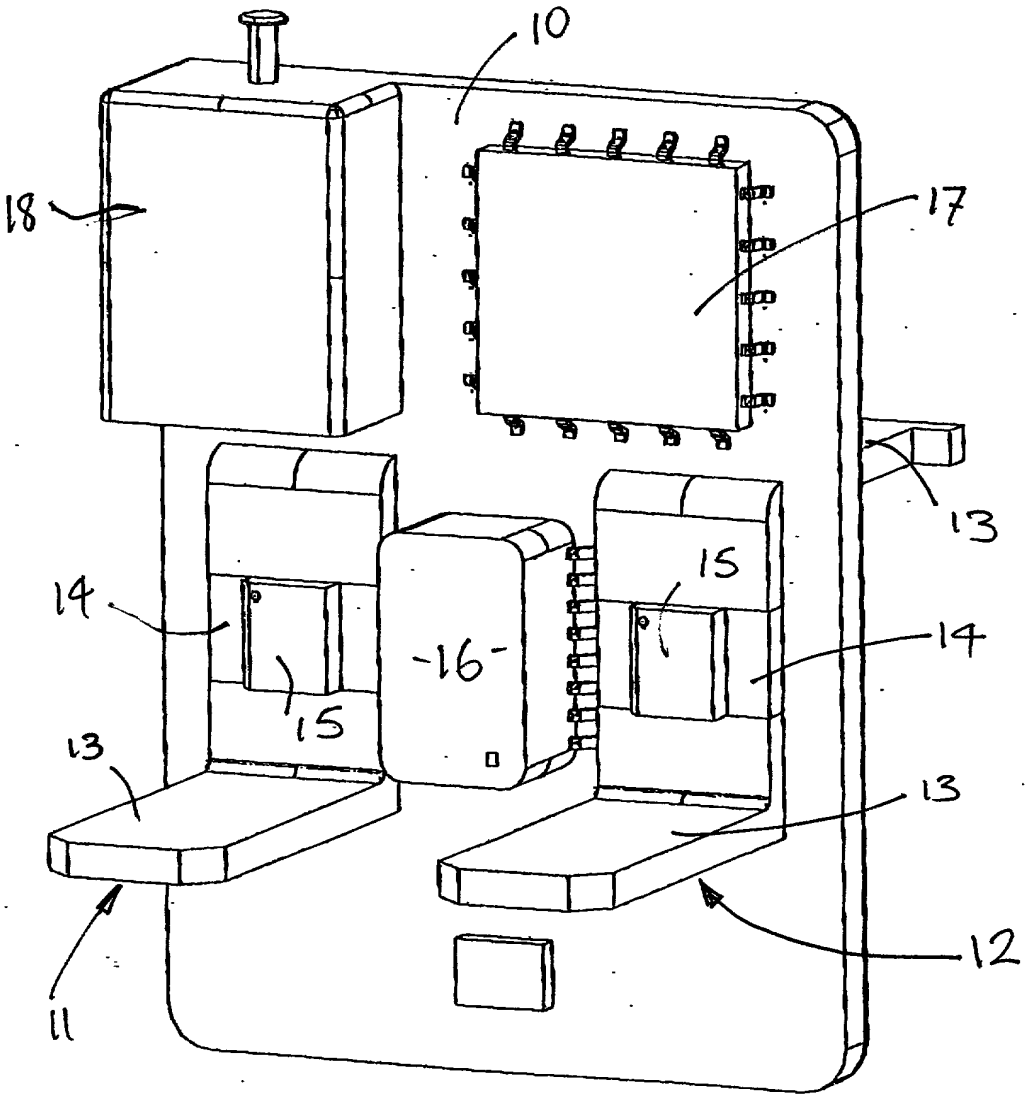

Fig 1

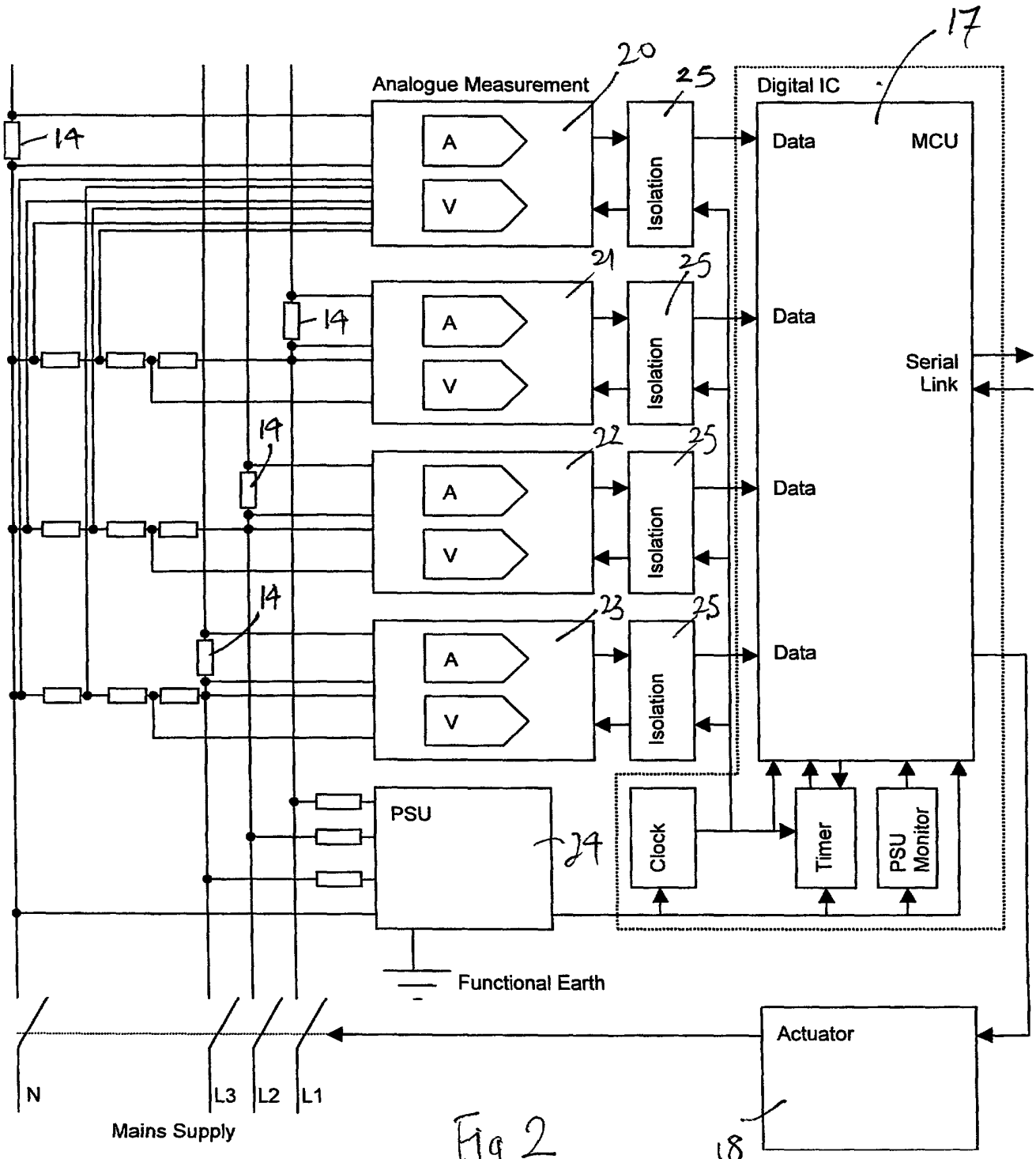
17
Analogue Measurement
20
25
Digital IC
14
A
V
Isolation
Data
MCU
21
Serial
Link
19
22
23
PSU
24
Clock
Timer
PSU
Monitor
Functional Earth
Actuator
18
N
L3
L2
L1
Mains Supply

Fig 2

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Docket No. 602985.1002

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **RESIDUAL CURRENT DETECTION DEVICE**, the specification of which

(check one) [X] is attached hereto.
[ ] was filed on _____ as Application Serial No. _____ and was amended on _____. (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, '1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, '119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application of patent for inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
9813982.7 (Number)	**Great Britain** (Country)	**30 June 1998** (Day/Month/Year Filed)	**[X]** Yes	[ ] No
GB99/02053 (Number)	**PCT** (Country)	**30 June 1999** (Day/Month/Year Filed)	**[X]** Yes	[ ] No

PRIOR PROVISIONAL APPLICATION(S)

I hereby claim the benefit under Title 35, United States Code, '119(e) of any United States provisional application(s) listed below.

_____ (Application Number) _____ (Filing Date)

_____ (Application Number) _____ (Filing Date)

I hereby claim the benefit under Title 35, United States Code, '120 of any United States application(s) listed below; insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, '112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, '1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____ (Application Serial No.)	_____ (Filing Date)	_____ (Status: patented, pending, abandoned)
_____ (Application Serial No.)	_____ (Filing Date)	_____ (Status: patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this

application and transact all business in the Patent and Trademark Office connected therewith:
George Gottlieb Reg. No. 22,035, Michael I. Rackman Reg. No. 20,639, James Reisman Reg. No. 22,007, Barry A. Cooper Reg. No. 28,725, Jeffrey M. Kaden Reg. No. 31,268, Tiberiu Weiss Reg. No. 29,876 J. David Dainow Reg. No. 22,959

SEND CORRESPONDENCE TO: **Gottlieb, Rackman & Reisman, P.C.**
270 Madison Avenue, New York
New York 10016-0601
USA

DIRECT TELEPHONE CALLS TO:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application of any patent issued thereon.

Full name of sole or first inventor **Robert Charles SKERRITT**

Inventor's signature _____

Residence **Penrhyn Bay, Conwy, United Kingdom** GBX

Citizenship **British**

Post Office Address **2 Charleston Close, Penrhyn Bay, Conwy, LL30 3HX, United Kingdom**

Full name of second joint inventor, if any **Mark David CROSIER**

Inventor's signature _____

Residence **Holyhead, Isle of Anglesey, United Kingdom** GBX

Citizenship **British**

Post Office Address **4 Sunrise Terrace, Gors Avenue, Holyhead, Isle of Anglesey, LL65 1PD, United Kingdom**

Full name of third joint inventor, if any **Martin Anthony MURRAY**

Inventor's signature _____

Residence **Bangor, United Kingdom** GBX

Citizenship **British**

Post Office Address **47 Penrhos Road, Bangor, LL57 2AX, United Kingdom**

Full name of fourth joint inventor, if any **Brian Martin REEDER**

Inventor's signature _____

Residence **Treaddur Bay, Isle of Anglesey, United Kingdom** GBX

Citizenship **British**

Post Office Address **'Samona', Lon Crecrist, Treaddur Bay, Isle of Anglesey, LL65 2AZ, United Kingdom**

Full name of fifth joint inventor, if any _____

Inventor's signature _____

Residence _____

Citizenship _____

Post Office Address _____